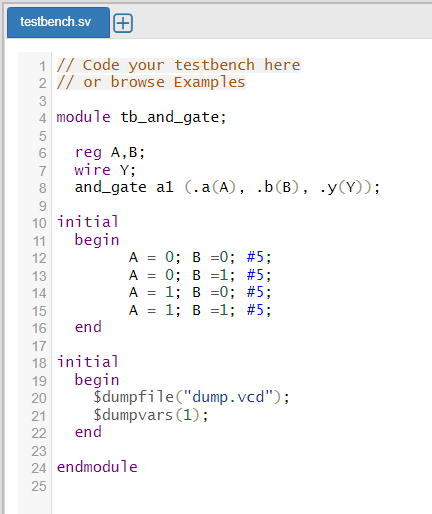
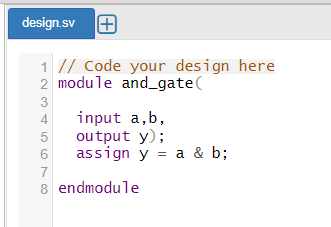
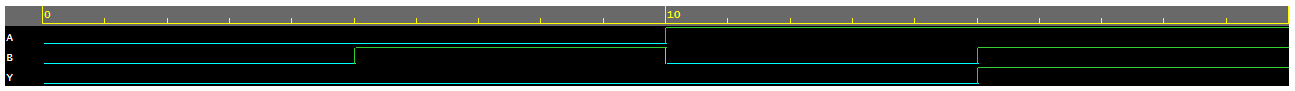
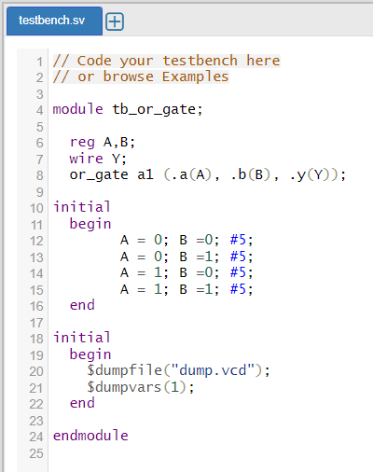
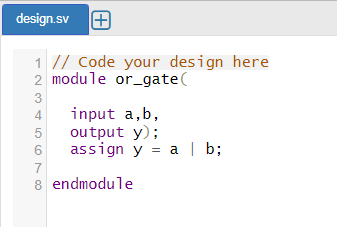
**Lab 2: Introduction To Verilog**

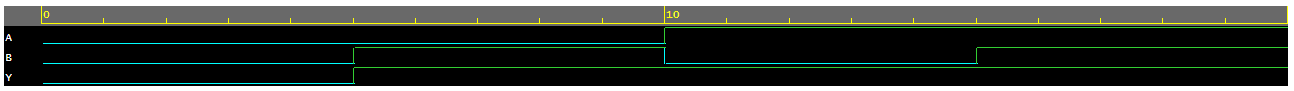
**Question 1: Write a Verilog code to implement AND gate. Write the corresponding Testbench code for the verification of your Verilog code**

** **

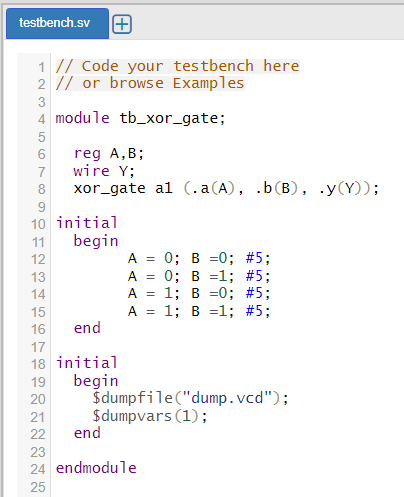
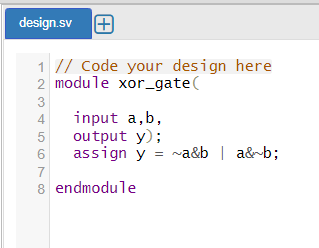
****

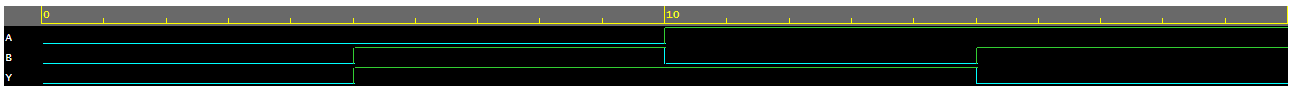
**Question 2: Write a Verilog code to implement OR gate. Write the corresponding Testbench code for the verification of your Verilog code.**

 ****

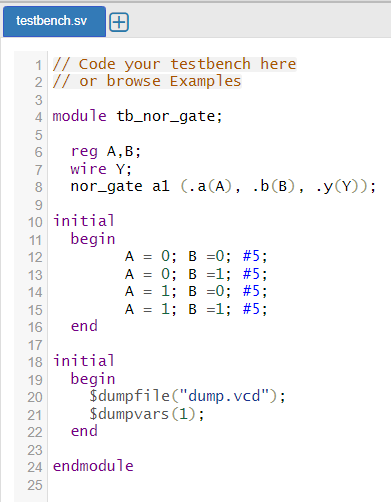
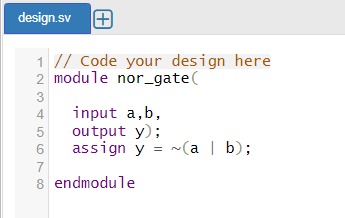
****

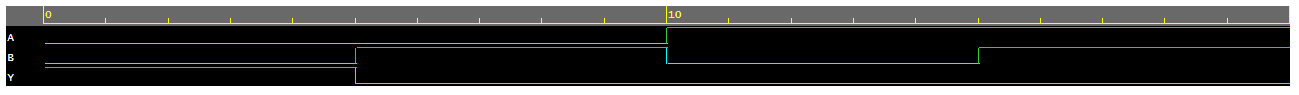
**Question 3:** **Write a Verilog code to implement XOR gate. Write the corresponding Testbench code for the verification of your Verilog code.**

** **

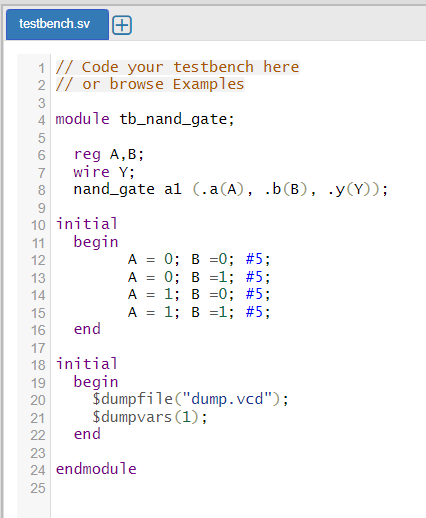
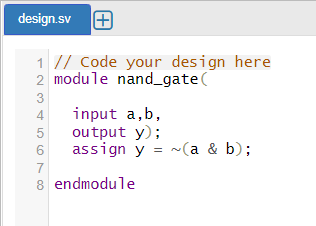
****

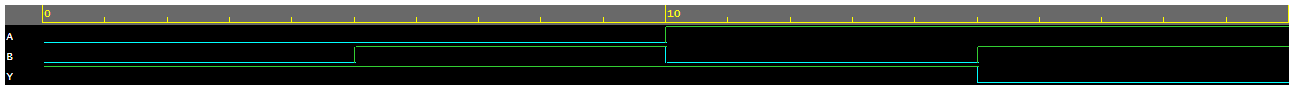
**Question 4: Write a Verilog code to implement NOR gate. Write the corresponding Testbench code for the verification of your Verilog code.**

** **

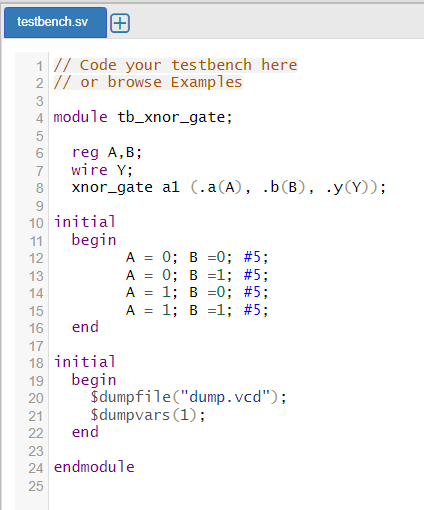
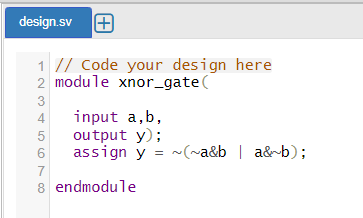
****

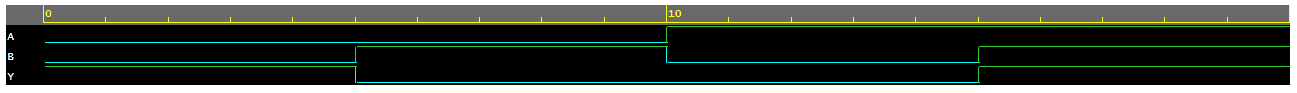
**Question 5: Write a Verilog code to implement NAND gate. Write the corresponding Testbench code for the verification of your Verilog code.**

** **

****

**Question 6: Write a Verilog code to implement XNOR gate. Write the corresponding Testbench code for the verification of your Verilog code**

** **

****